FIG. 1A

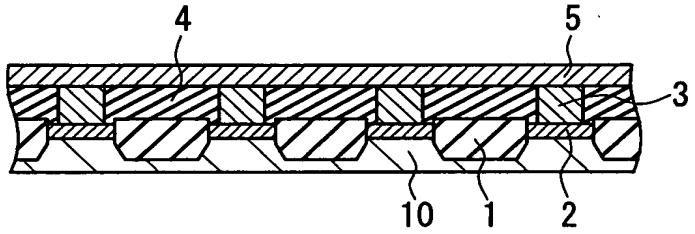


FIG. 1B

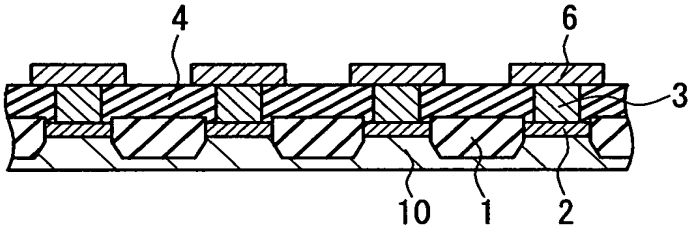


FIG. 1C

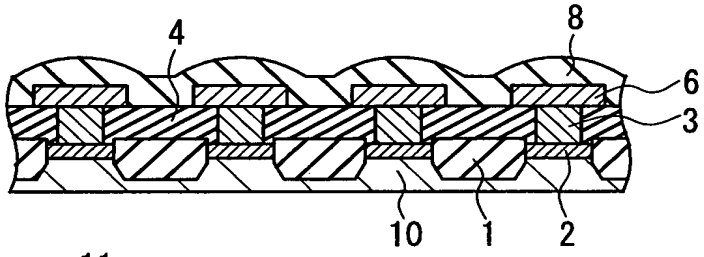


FIG. 1D

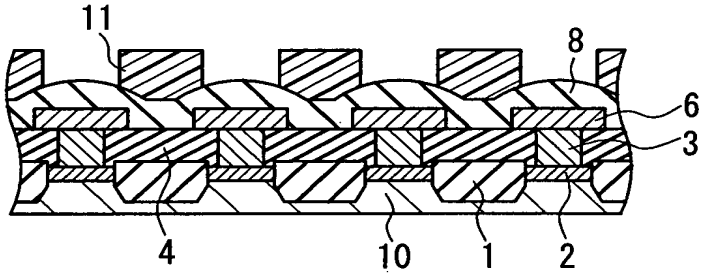


FIG. 1E

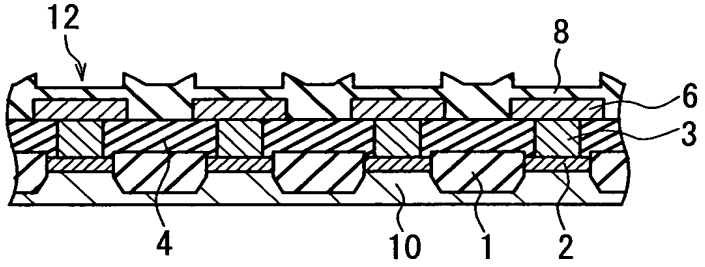


FIG. 1F

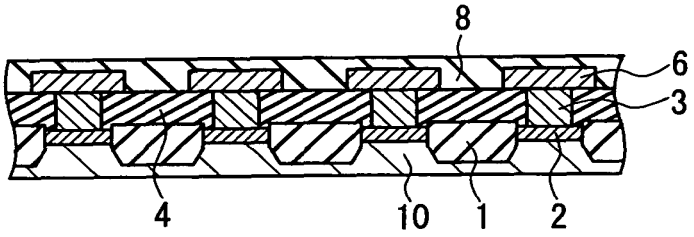


FIG. 1G

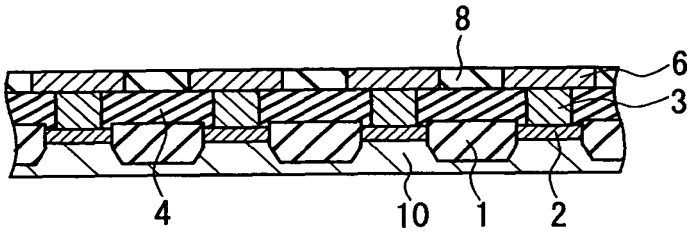


FIG. 1H

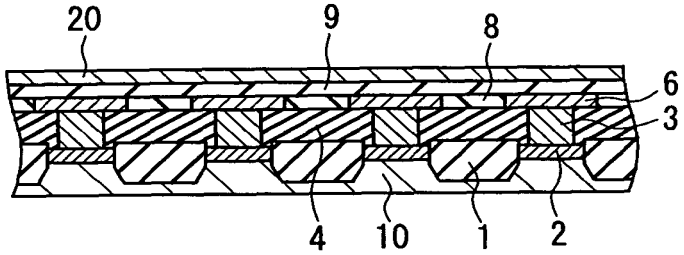


FIG. 1I

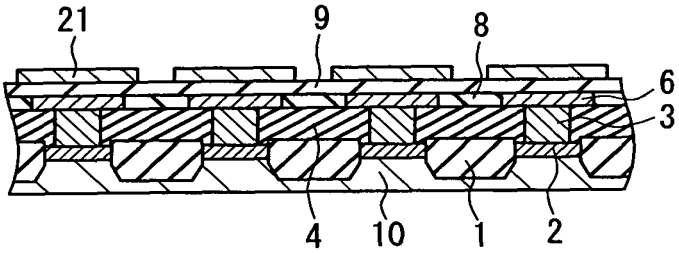


FIG. 1J

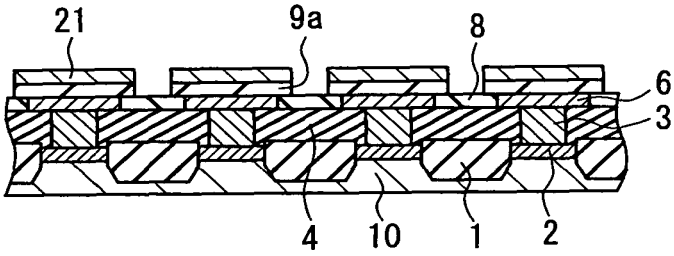


FIG. 2A

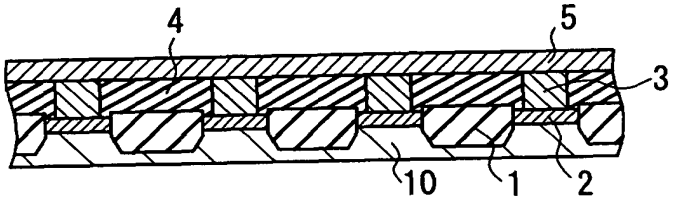


FIG. 2B

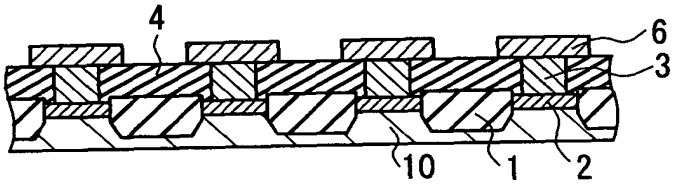


FIG. 2C

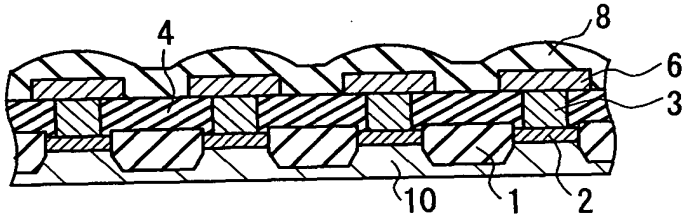


FIG. 2D

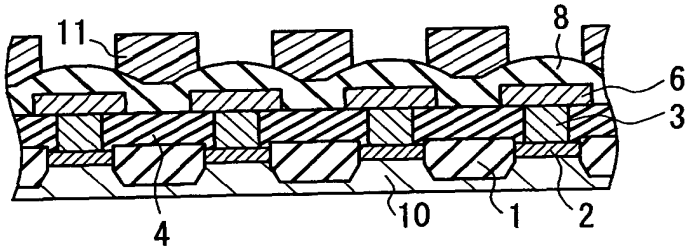


FIG. 2E

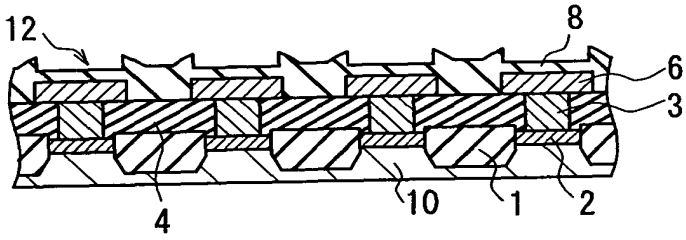


FIG. 2F

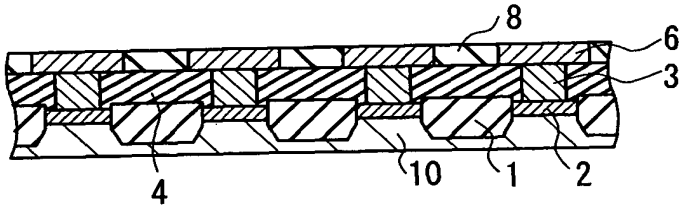


FIG. 3Aa

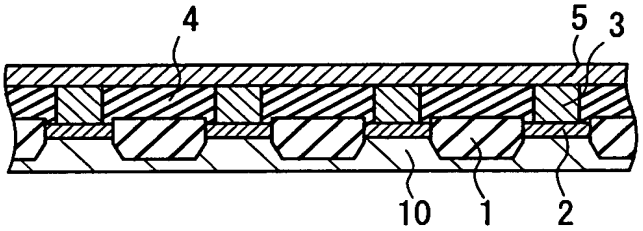


FIG. 3Ab

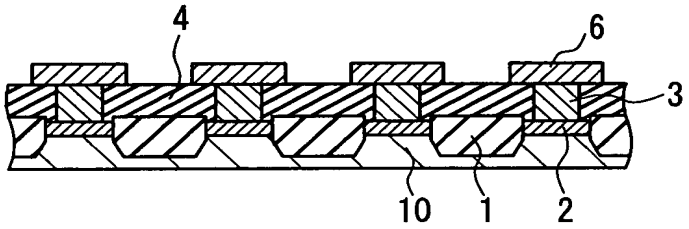


FIG. 3Ac

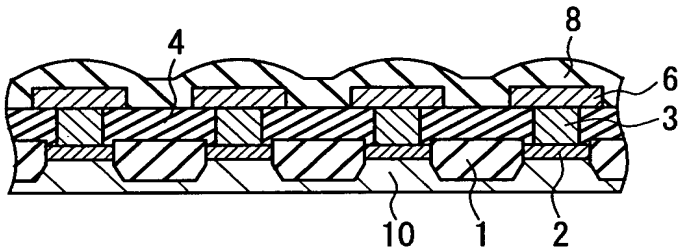


FIG. 3Ad

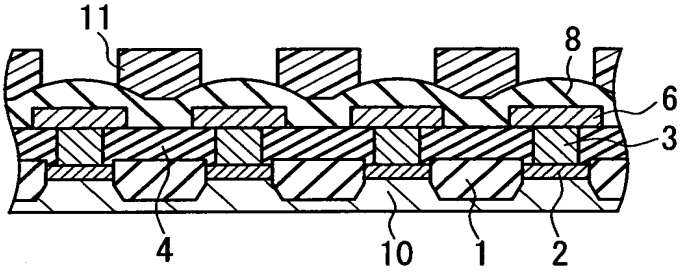


FIG. 3Ae

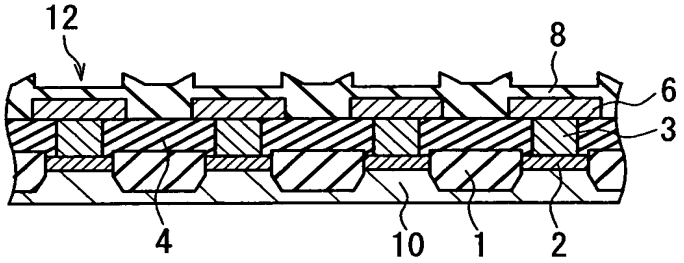


FIG. 3Af

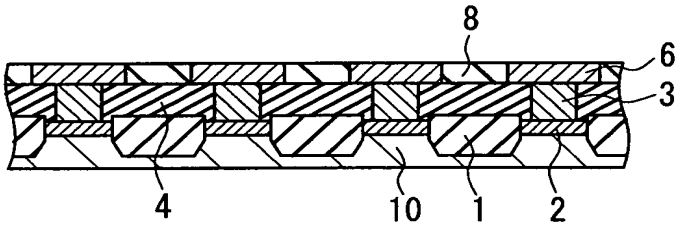


FIG. 3Ba

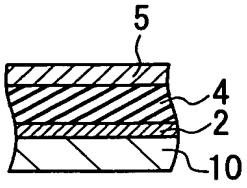


FIG. 3Bb

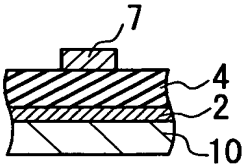


FIG. 3Bc

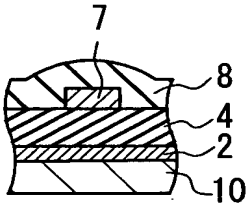


FIG. 3Bd

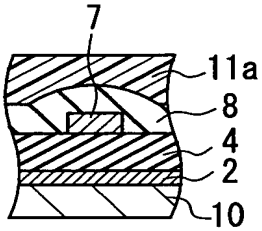


FIG. 3Be

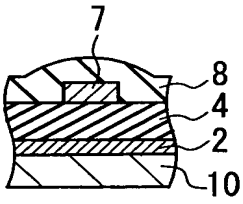


FIG. 3Bf

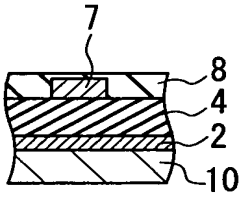


FIG. 4A

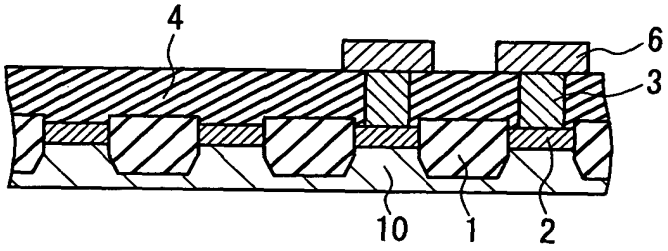


FIG. 4B

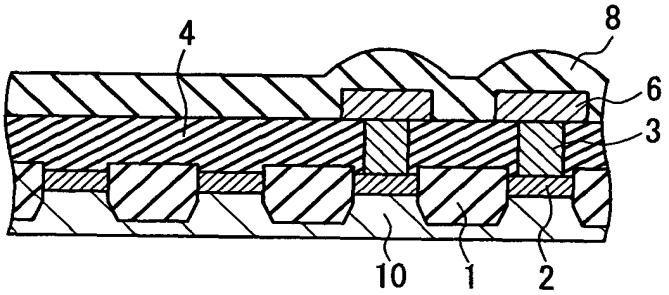


FIG. 4C

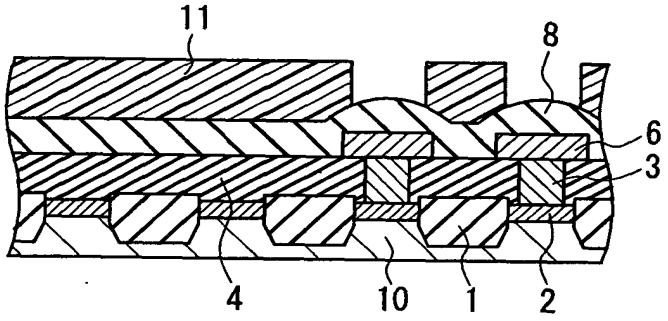


FIG. 4D

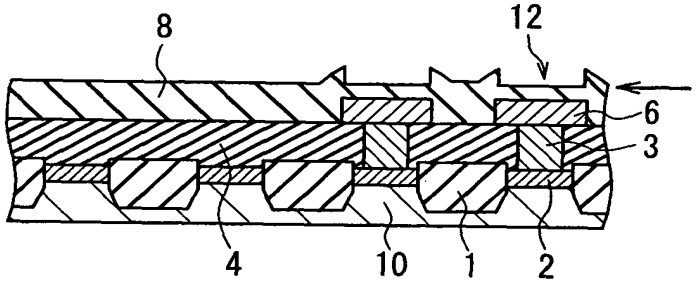


FIG. 4E

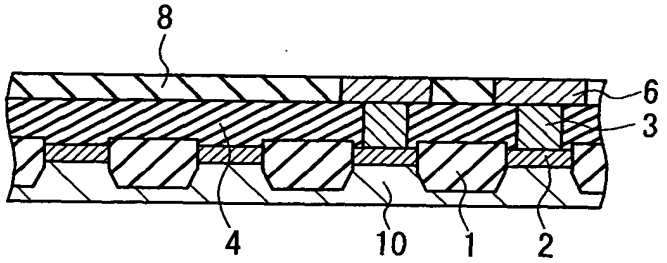


FIG. 5A

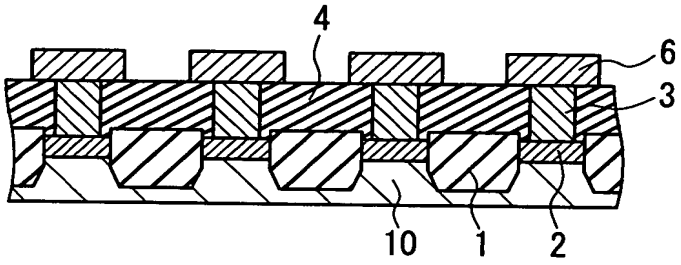


FIG. 5B

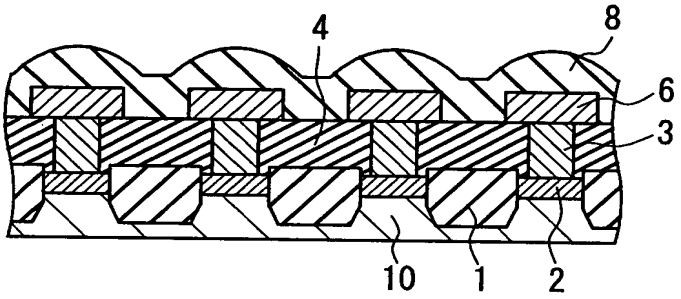


FIG. 5C

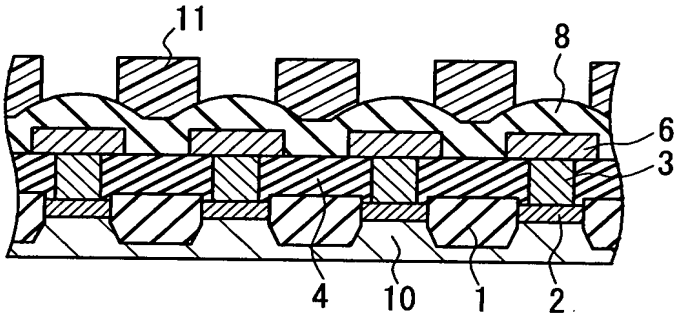


FIG. 5D

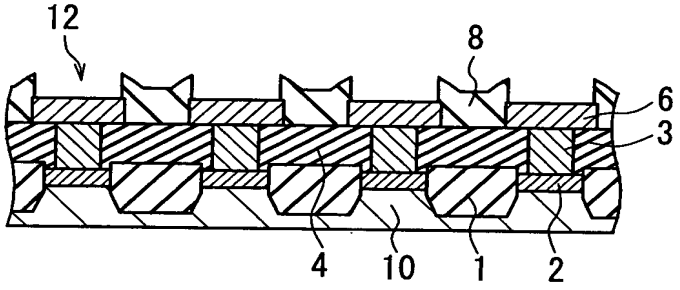


FIG. 5E

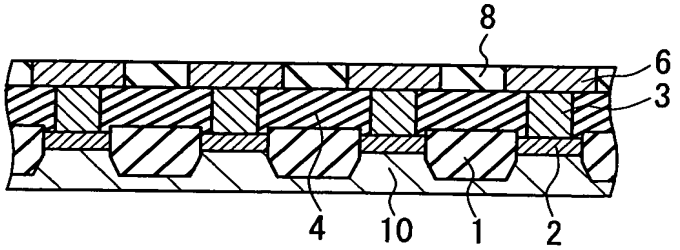


FIG. 6A

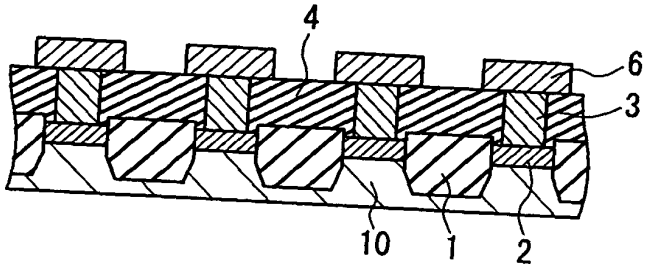


FIG. 6B

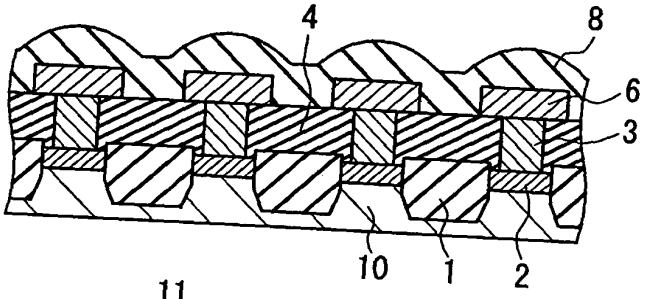


FIG. 6C

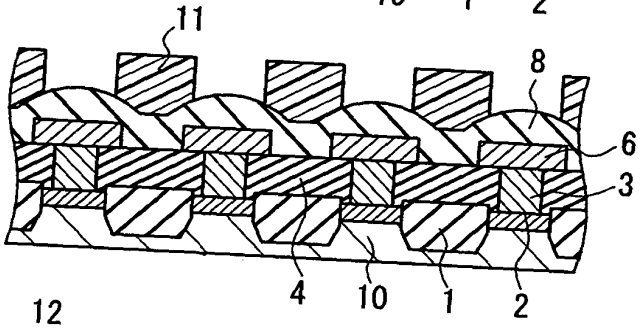


FIG. 6D

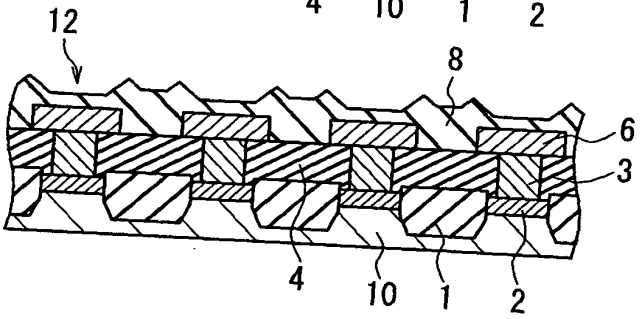


FIG. 6E

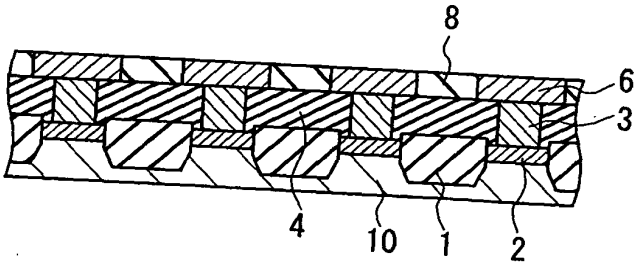


FIG. 7A

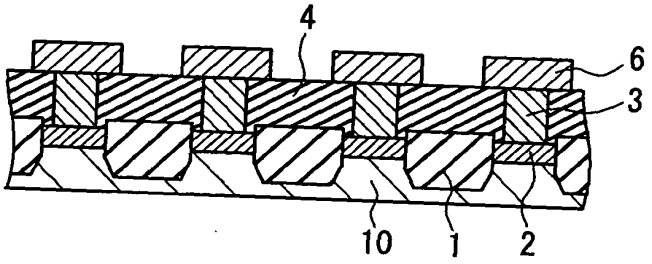


FIG. 7B

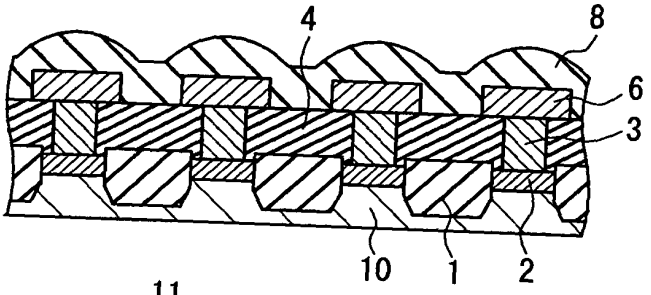


FIG. 7C

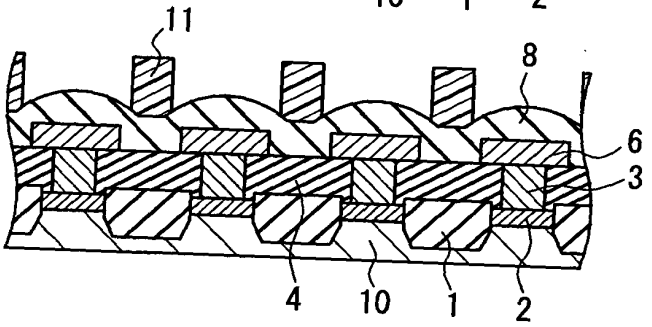


FIG. 7D

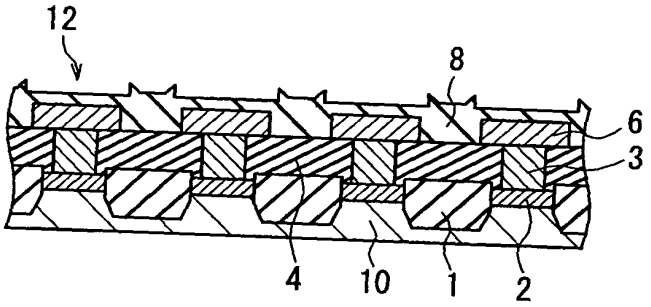


FIG. 7E

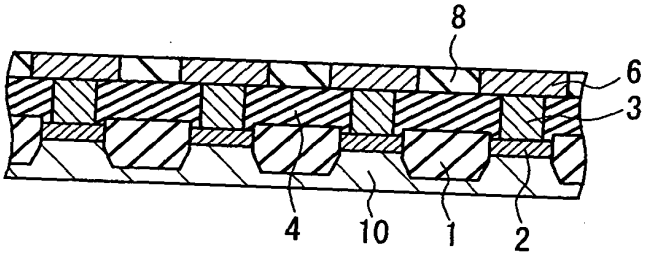


FIG. 8A

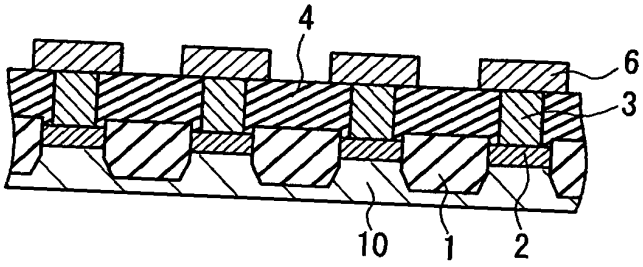


FIG. 8B

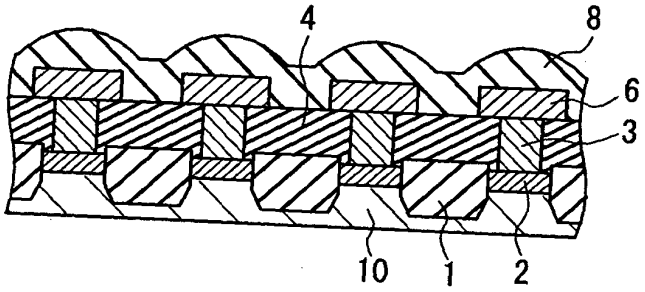


FIG. 8C

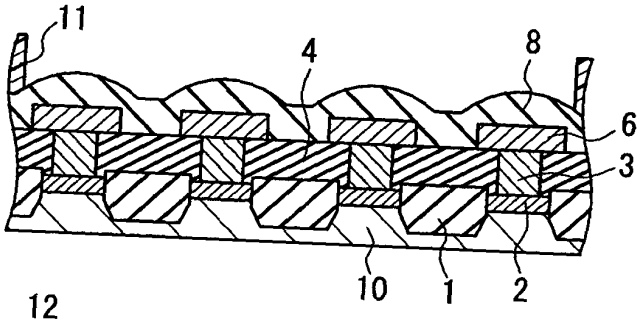


FIG. 8D

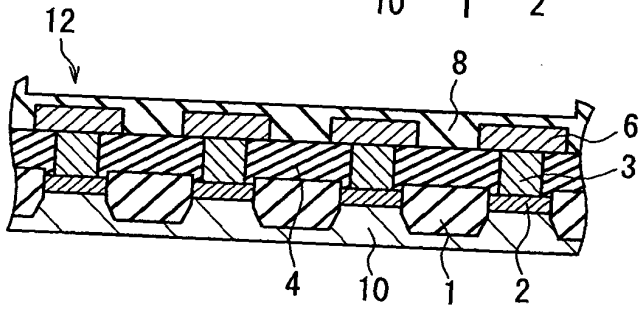


FIG. 8E

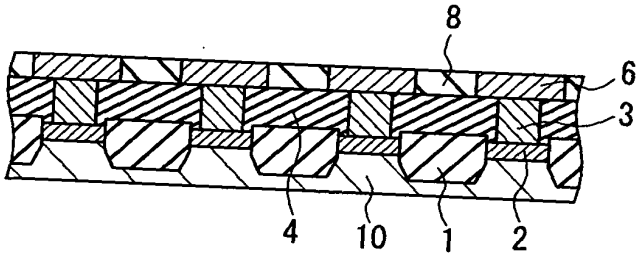


FIG. 9

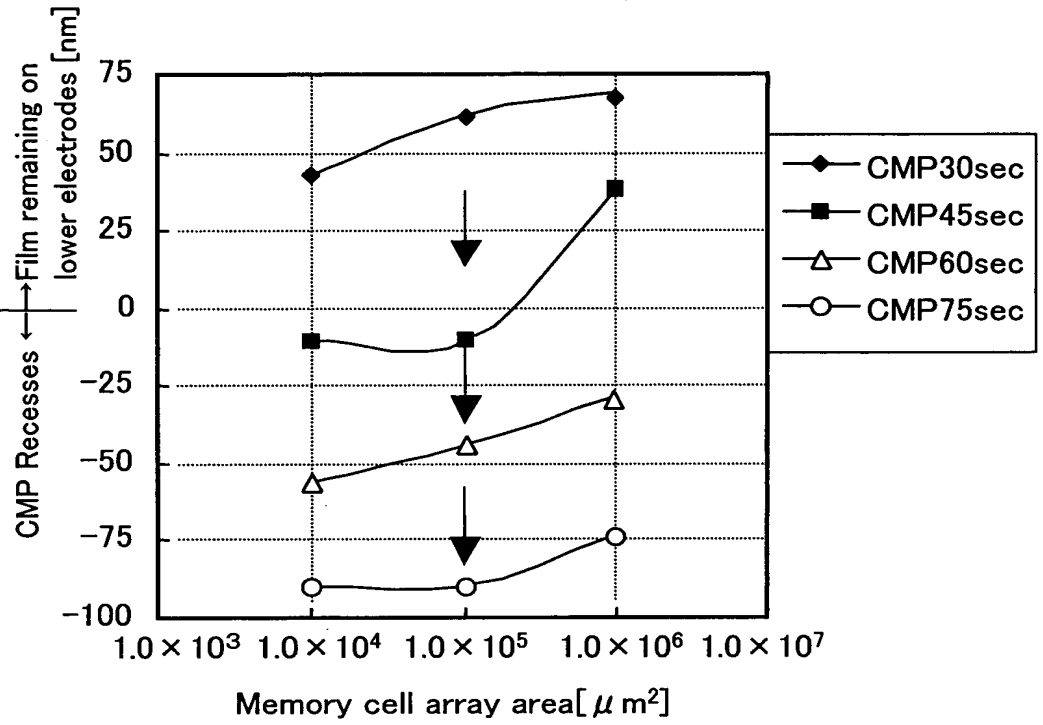

Film remaining on lower electrodes [nm]
CMP Recesses
75
50
25
0
−25
−50
−75
−100
1.0×10³ 1.0×10⁴ 1.0×10⁵ 1.0×10⁶ 1.0×10⁷
Memory cell array area[μm²]
CMP30sec
CMP45sec
CMP60sec
CMP75sec

FIG. 10

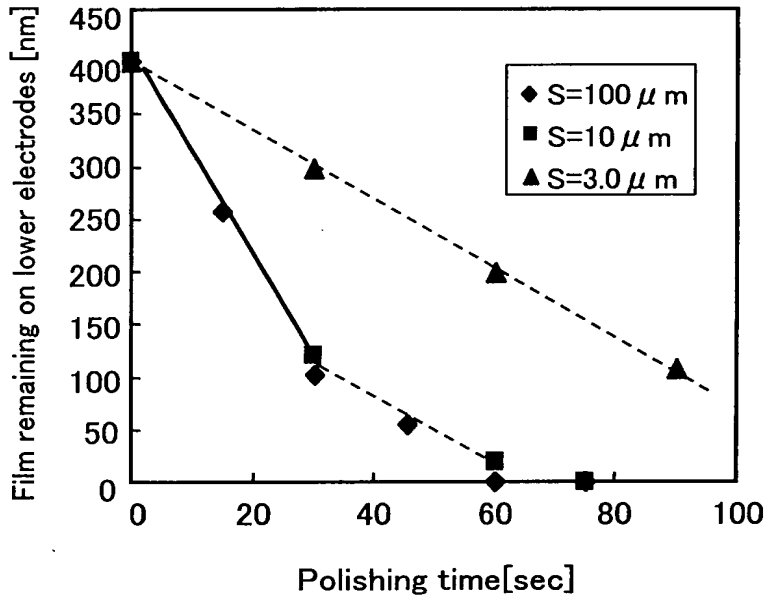

Film remaining on lower electrodes [nm]
450
400
350
300
250
200
150
100
50
0
0
20
40
60
80
100
Polishing time[sec]
S=100μm
S=10μm
S=3.0μm

FIG. 11A
PRIOR ART

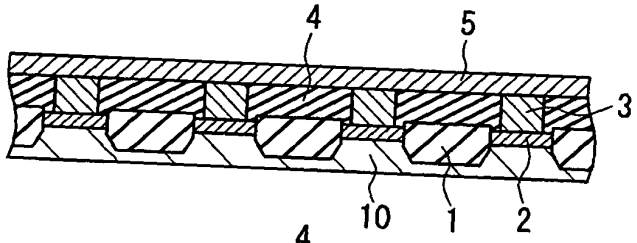


FIG. 11B
PRIOR ART

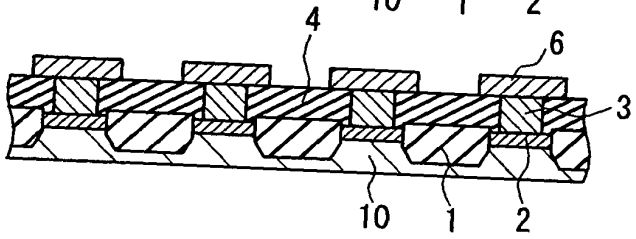


FIG. 11C
PRIOR ART

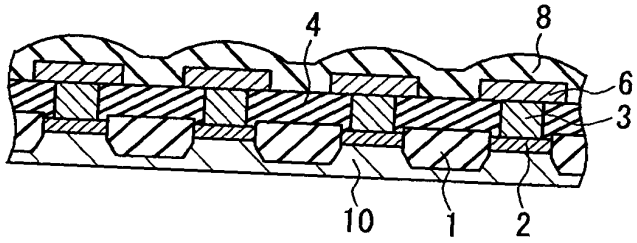


FIG. 11D
PRIOR ART

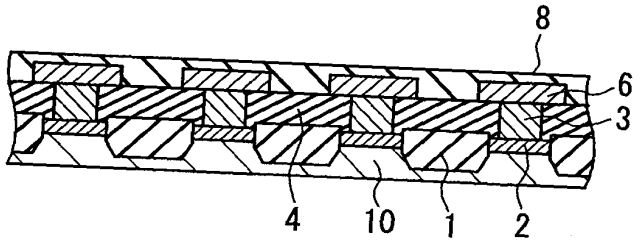


FIG. 11E
PRIOR ART

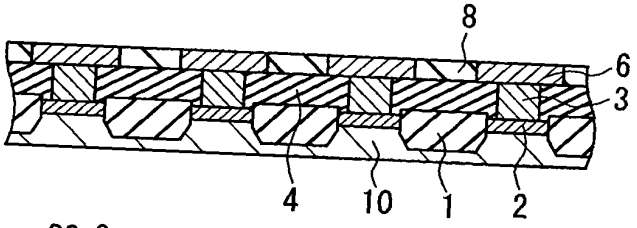


FIG. 11F
PRIOR ART

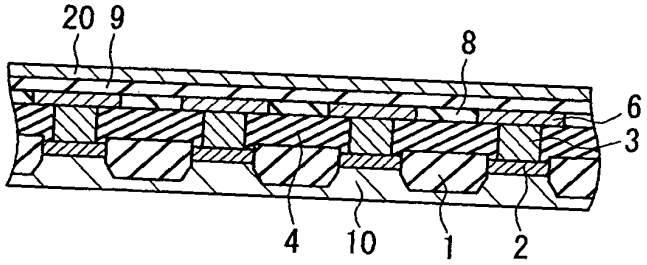


FIG. 12A
PRIOR ART

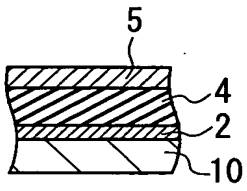


FIG. 12B
PRIOR ART

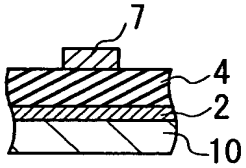


FIG. 12C
PRIOR ART

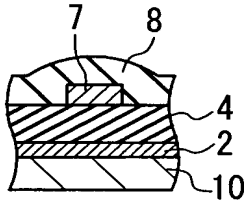


FIG. 12D
PRIOR ART

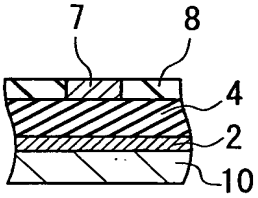
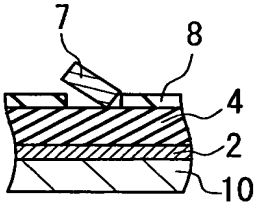


FIG. 12E
PRIOR ART



Larger memory cell array surface area

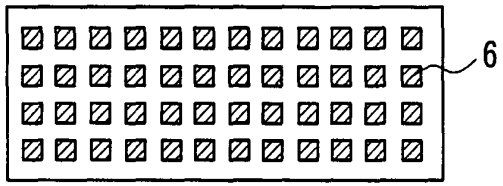


FIG. 13A1
PRIOR ART

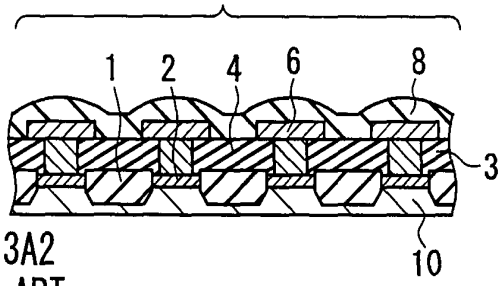


FIG. 13A2
PRIOR ART

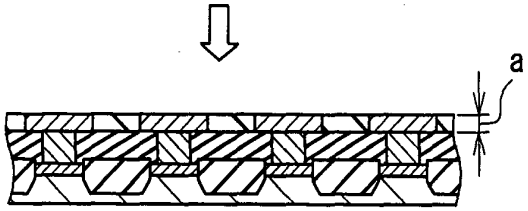


FIG. 13A3
PRIOR ART

Small memory cell array surface area

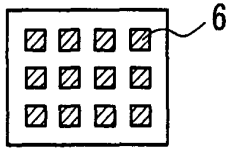


FIG. 13B1
PRIOR ART

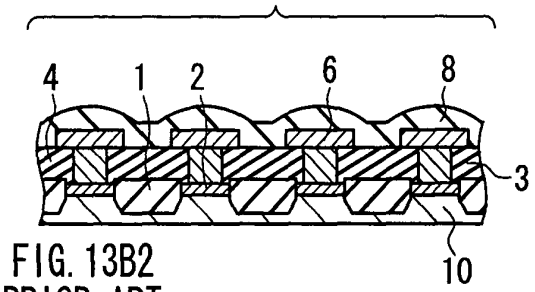


FIG. 13B2
PRIOR ART

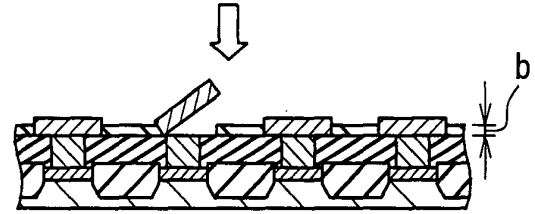


FIG. 13B3
PRIOR ART

Peripheral circuitry without lower electrodes

FIG. 13C1
PRIOR ART

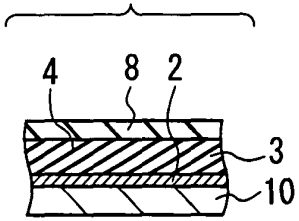


FIG. 13C2
PRIOR ART

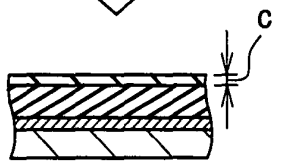


FIG. 13C3
PRIOR ART

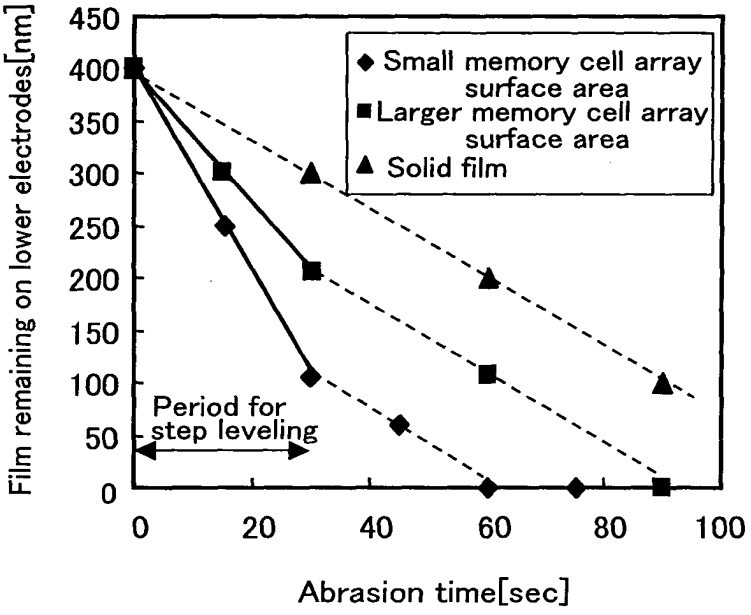


FIG. 14
PRIOR ART